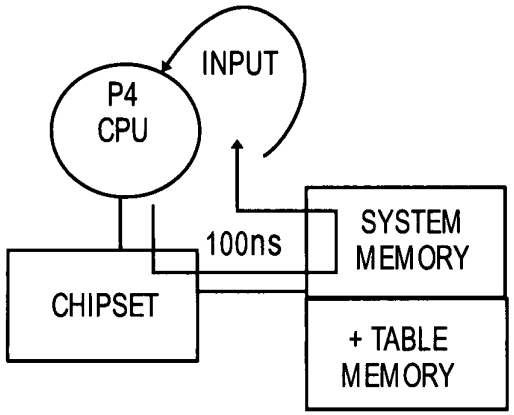
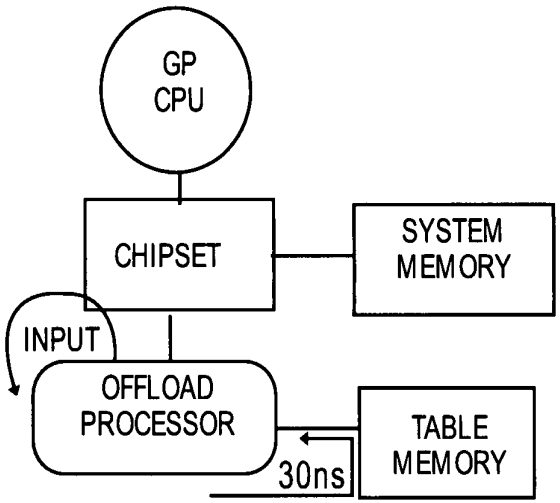
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	STORAGE: BOUND ON # OF STATES (FOR R CHARACTER REGULAR EXPRESSION)	EVALUATION TIME (FOR N BYTES OF INPUT) [ORDER OF]
DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	2^R (NEEDS VERY LARGE MEMORY)	**N** MEMORY ACCESS CYCLES
NON-DETERMINISTIC FINITE STATE AUTOMATA OR NFA RUNNING ON A GP CPU	**R**	**R * N** CPU CACHE+BRANCH CYCLES

FIG. 1A
(PRIOR ART)

CPU WALKING DFA TABLE IN DRAM



COPROCESSOR CLOSER TO TABLE IN SRAM



PERFORMANCE ON EVALUATING REGULAR EXPRESSIONS ON EVERY BYTE OF INPUT STREAM

1000s OF REs @ 100 Mbps

GIGABYTES OF MEMORY

100s OF REs @ 280 Mbps

100s OF MBs OF SRAM

FIG. 1B
(PRIOR ART)

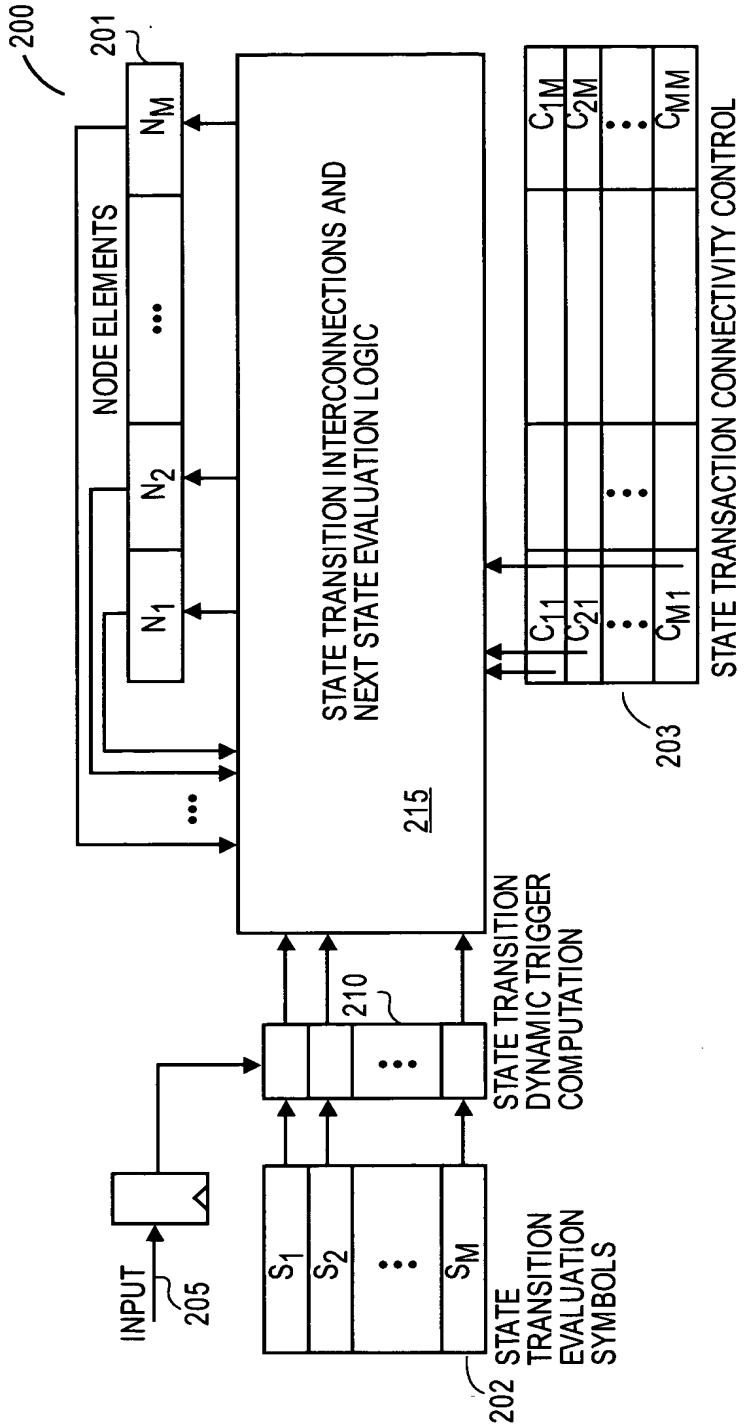

200
201
NODE ELEMENTS
N_M
N_2
N_1
STATE TRANSITION INTERCONNECTIONS AND NEXT STATE EVALUATION LOGIC
215
C_{1M}
C_{2M}
C_{MM}
C_{11}
C_{21}
C_{M1}
STATE TRANSACTION CONNECTIVITY CONTROL
203
210
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION
INPUT
205
S_1
S_2
S_M
202 STATE TRANSITION EVALUATION SYMBOLS

FIG. 2

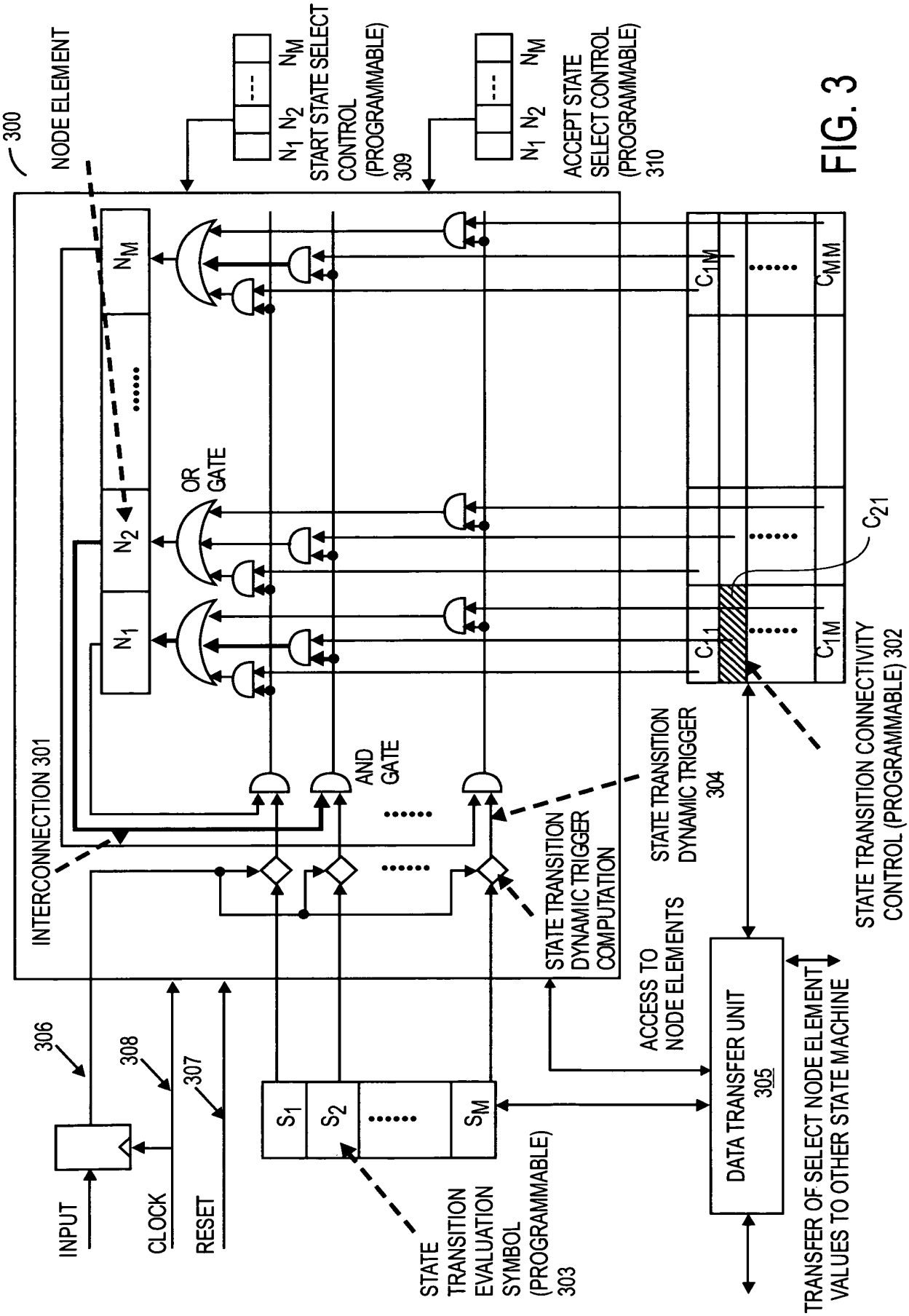

300
NODE ELEMENT
START STATE SELECT CONTROL (PROGRAMMABLE) 309
ACCEPT STATE SELECT CONTROL (PROGRAMMABLE) 310
N1 N2 NM
OR GATE
AND GATE
INTERCONNECTION 301
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION
STATE TRANSITION DYNAMIC TRIGGER 304
STATE TRANSITION CONNECTIVITY CONTROL (PROGRAMMABLE) 302
C11
C1M
CM1
CMM
C21
ACCESS TO NODE ELEMENTS
DATA TRANSFER UNIT 305
TRANSFER OF SELECT NODE ELEMENT VALUES TO OTHER STATE MACHINE
306
308
307
INPUT
CLOCK
RESET
S1 S2 SM
STATE TRANSITION EVALUATION SYMBOL (PROGRAMMABLE) 303

FIG. 3

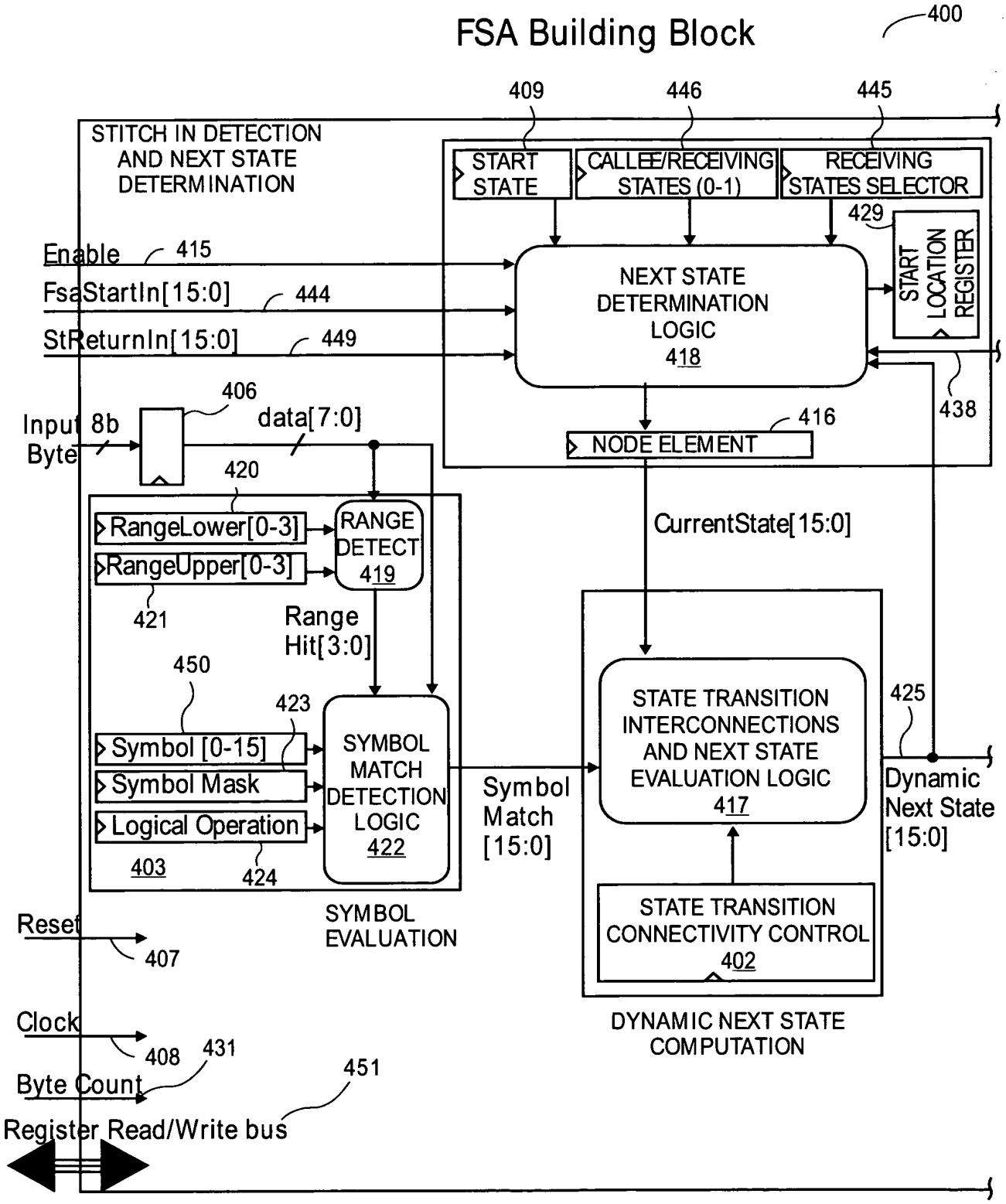

FSA Building Block
400
409
446
445
STITCH IN DETECTION AND NEXT STATE DETERMINATION
START STATE
CALLEE/RECEIVING STATES (0-1)
RECEIVING STATES SELECTOR
429
START LOCATION REGISTER
Enable
415
FsaStartIn[15:0]
444
StReturnIn[15:0]
449
NEXT STATE DETERMINATION LOGIC
418
438
406
Input 8b Byte
data[7:0]
416
NODE ELEMENT
420
RangeLower[0-3]
RangeUpper[0-3]
RANGE DETECT
419
421
Range Hit[3:0]
CurrentState[15:0]
450
423
Symbol [0-15]
Symbol Mask
Logical Operation
SYMBOL MATCH DETECTION LOGIC
422
403
424
SYMBOL EVALUATION
Symbol Match [15:0]
STATE TRANSITION INTERCONNECTIONS AND NEXT STATE EVALUATION LOGIC
417
425
Dynamic Next State [15:0]
STATE TRANSITION CONNECTIVITY CONTROL
402
DYNAMIC NEXT STATE COMPUTATION
Reset
407
Clock
408
431
Byte Count
451
Register Read/Write bus

FIG. 4

FSA Building Block

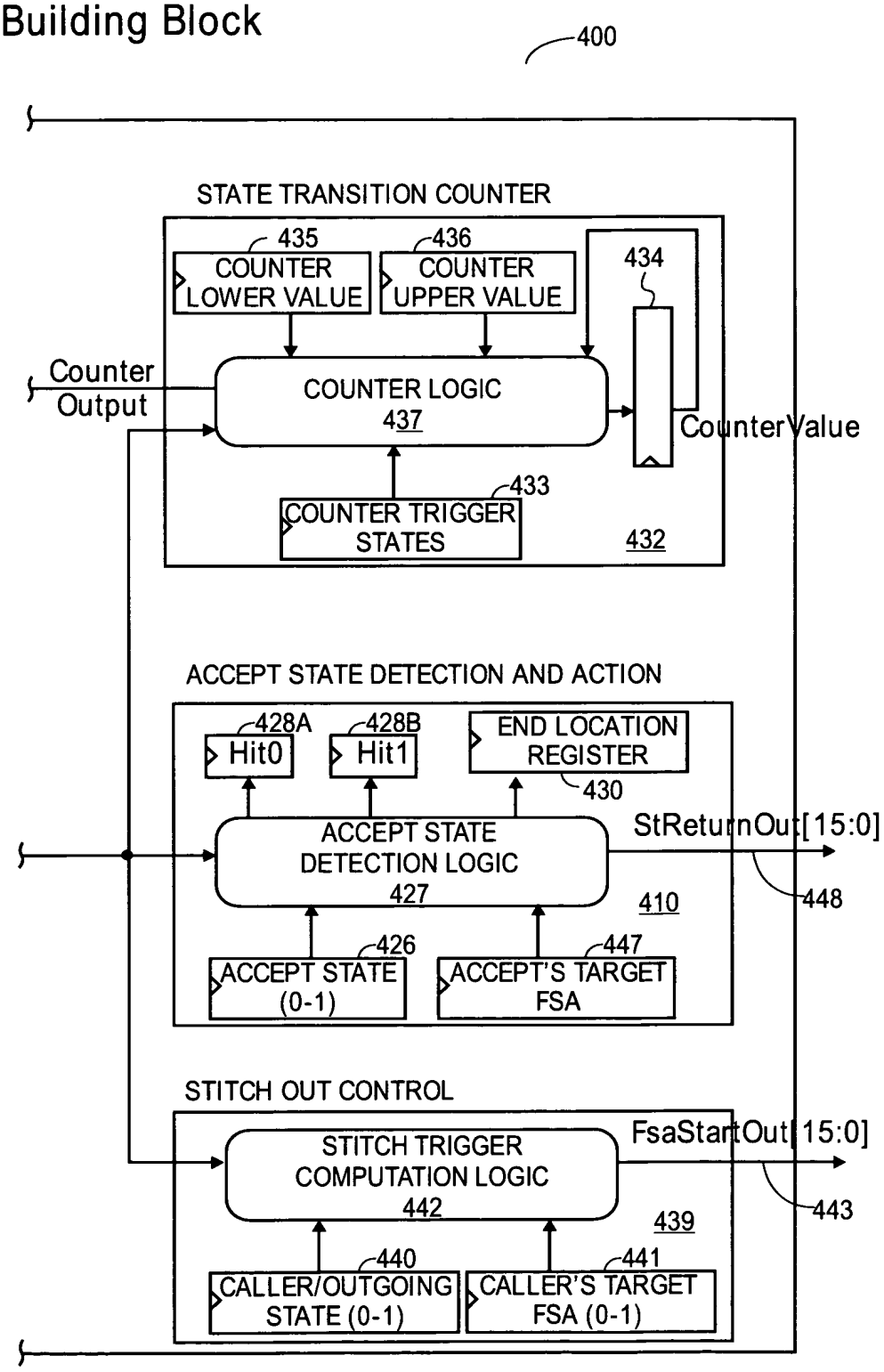


FIG. 4 (CONT.)

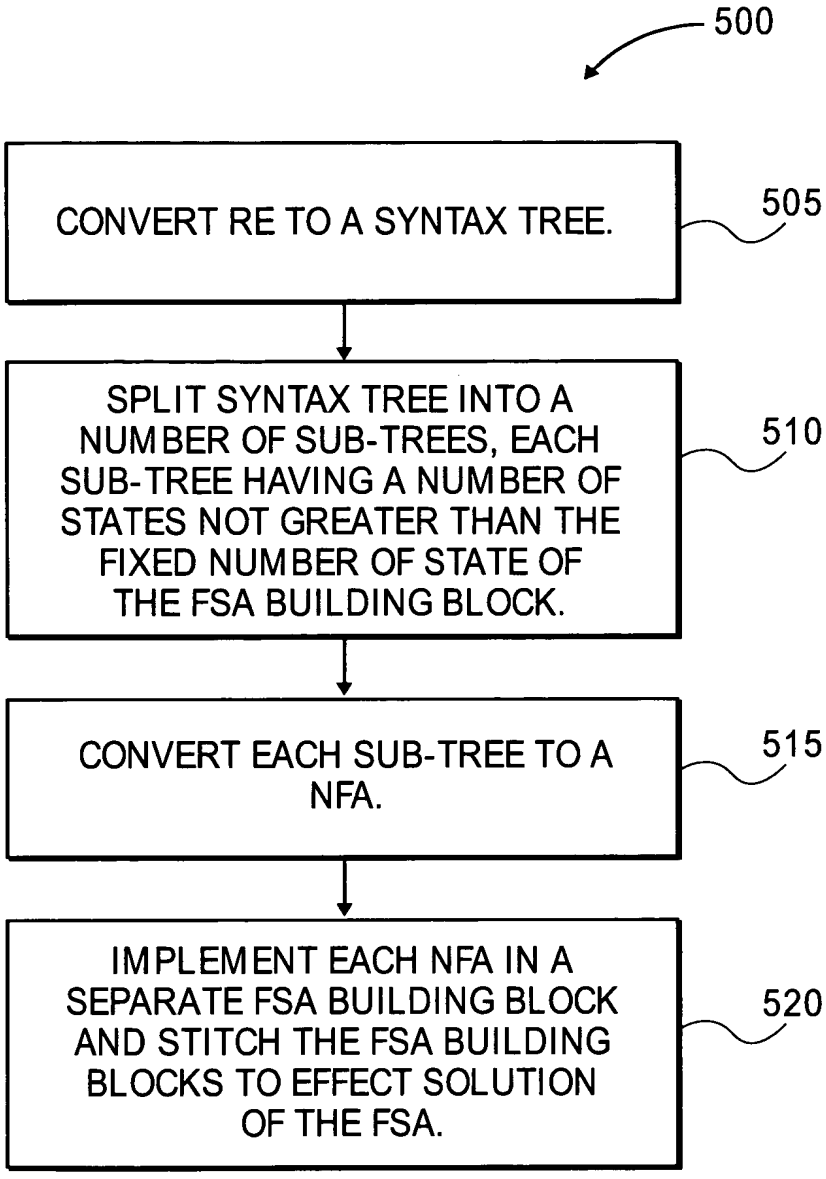

500
CONVERT RE TO A SYNTAX TREE.
505
SPLIT SYNTAX TREE INTO A NUMBER OF SUB-TREES, EACH SUB-TREE HAVING A NUMBER OF STATES NOT GREATER THAN THE FIXED NUMBER OF STATE OF THE FSA BUILDING BLOCK.
510
CONVERT EACH SUB-TREE TO A NFA.
515
IMPLEMENT EACH NFA IN A SEPARATE FSA BUILDING BLOCK AND STITCH THE FSA BUILDING BLOCKS TO EFFECT SOLUTION OF THE FSA.
520

FIG. 5

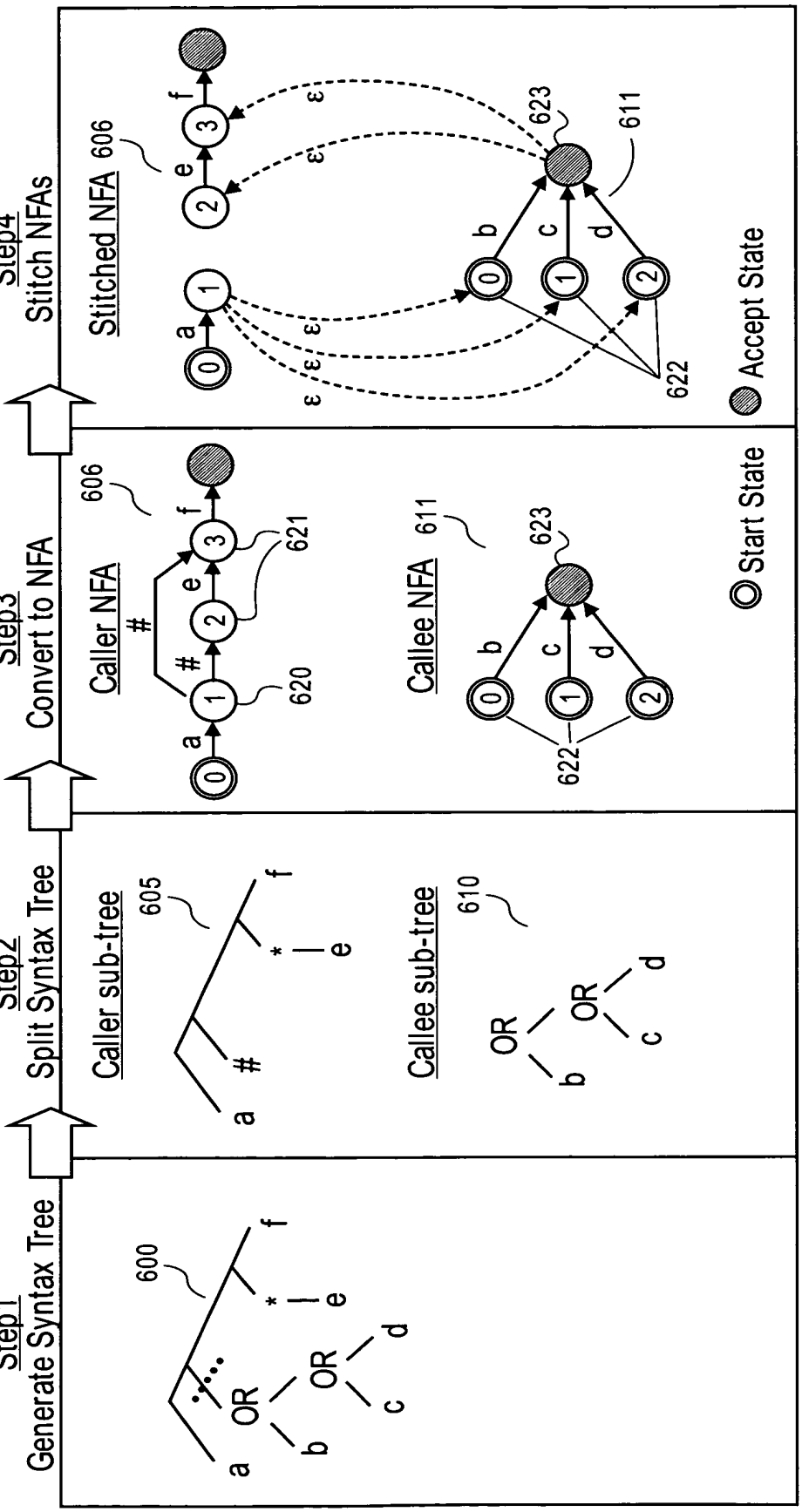


FIG. 6A FIG. 6B FIG. 6C FIG. 6D

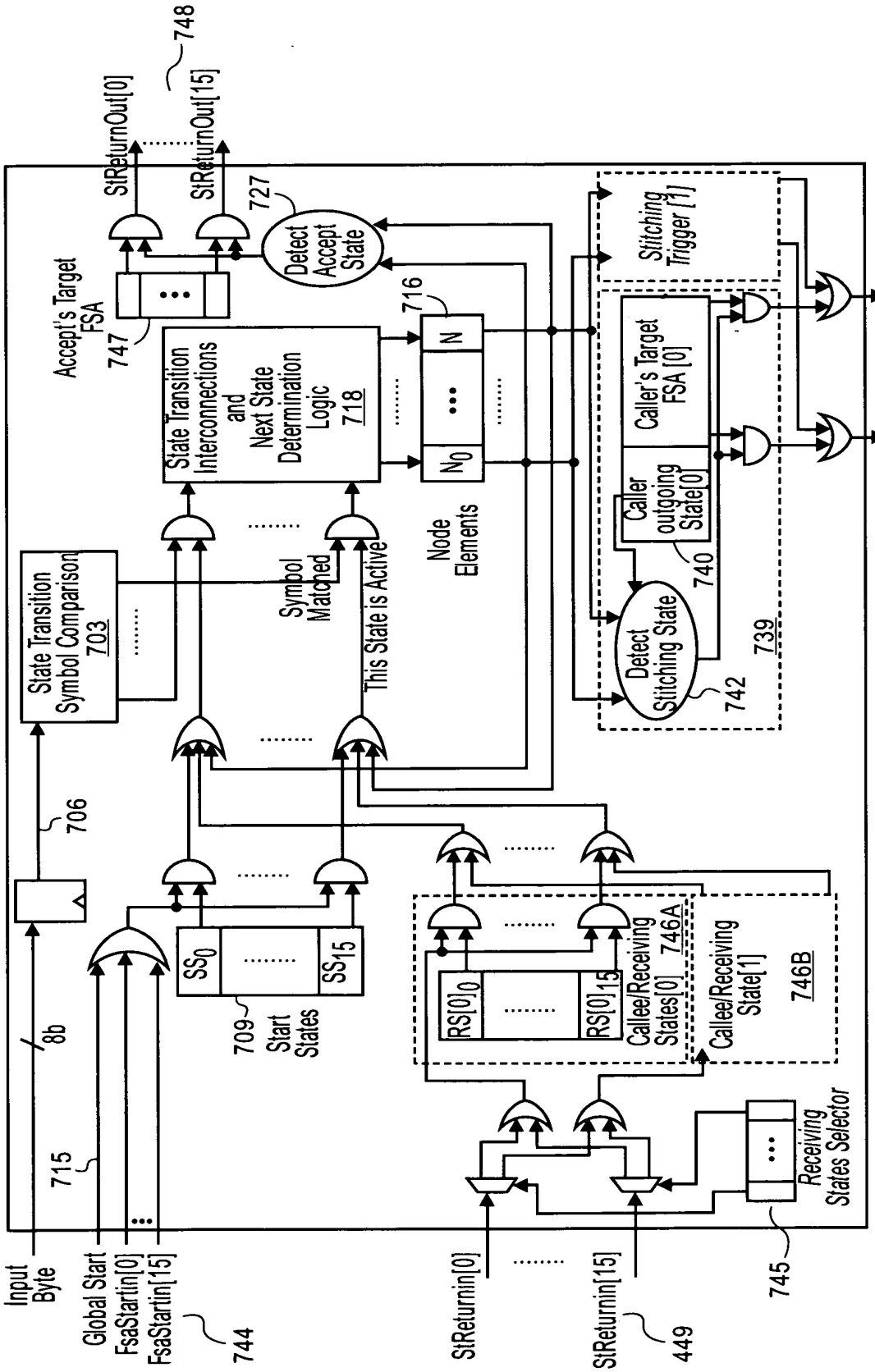

StReturnOut[0]
StReturnOut[15]
748
727
Detect Accept State
Accept's Target FSA
747
State Transition Interconnections and Next State Determination Logic 718
716
N
N0
Node Elements
Stitching Trigger [1]
Caller's Target FSA [0]
Caller outgoing State[0]
740
Detect Stitching State
742
739
743
FsaStartOut[15]
FsaStartOut[0]
State Transition Symbol Comparison 703
Symbol Matched
This State is Active
706
8b
715
SS0
SS15
709
Start States
RS[0]0
RS[0]15
Callee/Receiving States[0] 746A
Callee/Receiving State[1] 746B
Receiving States Selector
745
Input Byte
Global Start FsaStartin[0]
FsaStartin[15]
744
StReturnin[0]
StReturnin[15]
449

FIG. 7

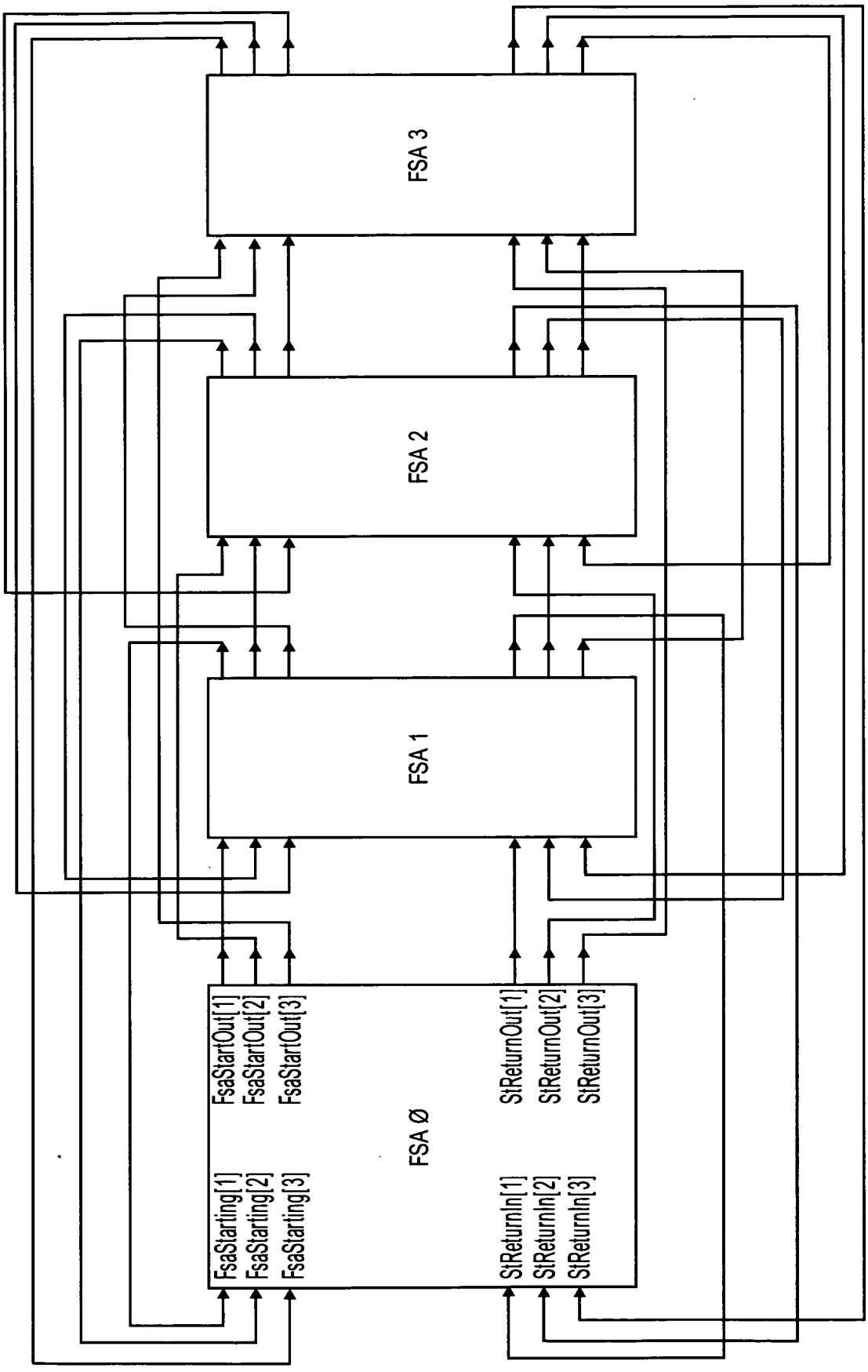

FSA 3
FSA 2
FSA 1
FSA Ø
FsaStartOut[1]
FsaStartOut[2]
FsaStartOut[3]
FsaStarting[1]
FsaStarting[2]
FsaStarting[3]
StReturnOut[1]
StReturnOut[2]
StReturnOut[3]
StReturnIn[1]
StReturnIn[2]
StReturnIn[3]

FIG. 8

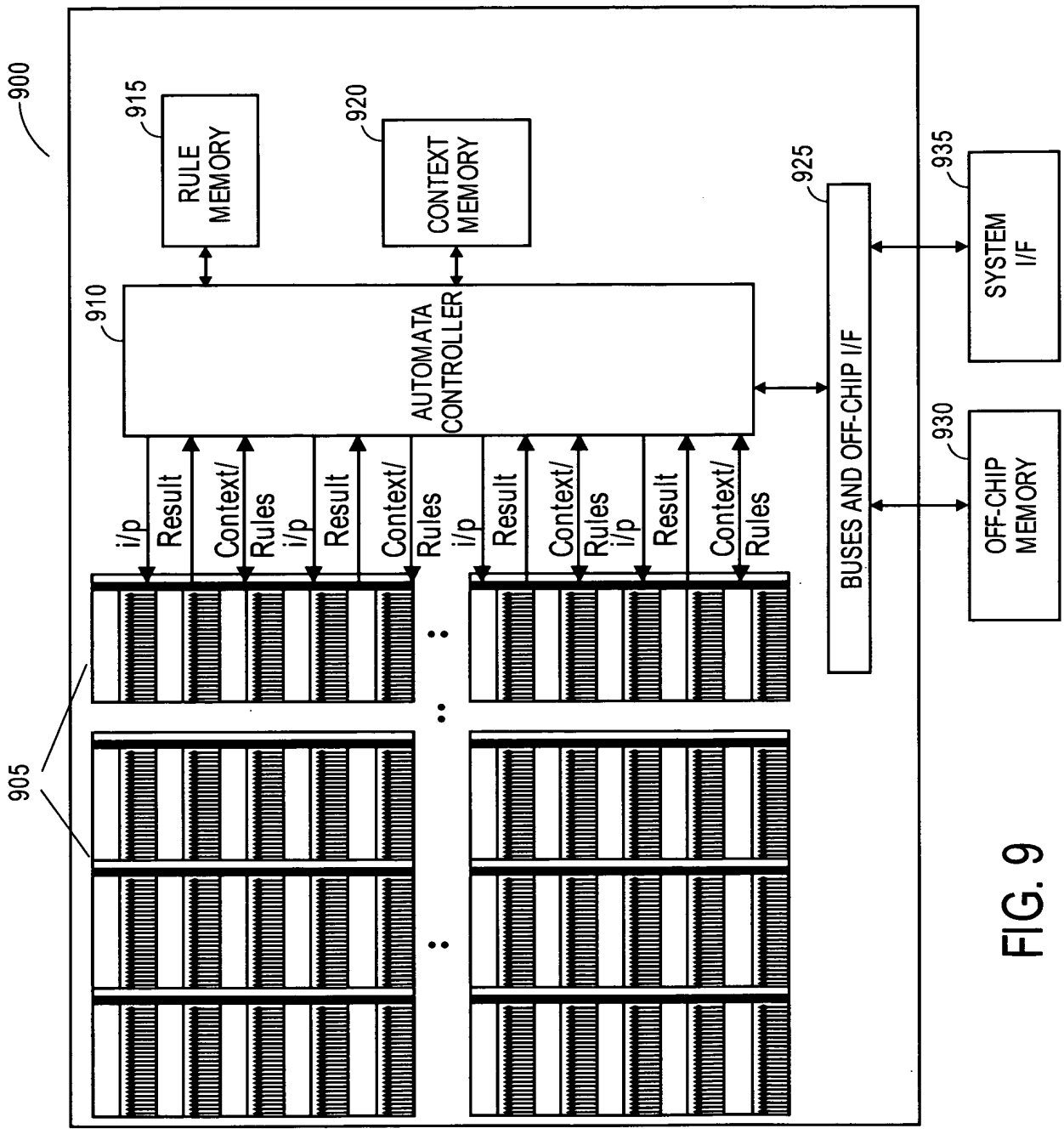

900
915
RULE MEMORY
920
CONTEXT MEMORY
925
935
SYSTEM I/F
910
AUTOMATA CONTROLLER
BUSES AND OFF-CHIP I/F
930
OFF-CHIP MEMORY
i/p
Result
Context/ Rules
905

FIG. 9